

Analysis and Design of Low Power High Speed Dynamic Latch Comparator using CMOS Process

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Abstract— This paper presents the need for ultra low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18- μm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.5 V and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153 μW , respectively.

Index Terms— Double tail Comparator, high speed analog-to-digital converters, dynamic regenerative comparators, conventional double tail comparator, CMOS, intuition, Post-layout simulation.

I. INTRODUCTION

1.1 OVERVIEW

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs such as flash ADCs, require high-speed, low power comparators. High-speed comparators in Ultra Deep Sub Micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply Voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range[8], which is important in many high-speed ADC architectures, such as flash ADCs.

1.2 A YIELD-OPTIMIZED LATCH-TYPE SRAM SENSE AMPLIFIER

A yield analysis of a latch-type voltage sense amplifier with a high-impedance differential input stage is presented. It quantifies the impact of supply voltage, input DC level, transistor sizing and temperature on the input offset voltage. The input dc level turns out to be most significant. Also an analytical expression for the sensing delay is derived. Experimental results in 130nm CMOS confirm that the yield can be significantly improved by lowering the input dc voltage to about 70% of the supply voltage[1]. Thereby, the offset standard deviation decreases from 19mV to 8.5mV without effecting the delay which is measured to be 119ps at 1.5V supply point ($V(\text{SO}) = V(\text{SON})$). In the presence of mismatch and noise a wrong output signal can develop for small input voltage differences.

This paper investigates the design issues for this type of sense amplifier to ensure a fast and correct decision even for small input signals[10]. The transient behavior, shown in Fig.1.1 (at a large value of VDD for better visibility), consists of three phases. The enable signal EN starts the operation by turning on M9.

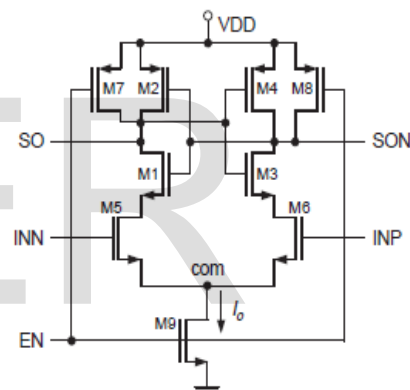


Fig. 1. Latch-type Voltage Sense Amplifier

So an increasing output difference develops. Now strong positive feedback enhances the output voltage difference starting from an initial value V_0 as marked. The latching completes during a third phase where one n-channel transistor is cut off. Then the current flow stops and the whole sense amplifier do not dissipate static power.

1.3 LOW-VOLTAGE OPERATIONAL AMPLIFIER

One of the most important basic building blocks in analog and mixed mode circuits is the operational amplifier. In a low-voltage (LV) Op-amp, the minimum supply value is imposed by the differential pair of the input stage and is equal to the threshold voltage (V_{th}) plus two overdrive voltages (V_{Dsat}). In typical CMOS processes, this value turns out to be around 1V. On the other hand, the main limitation of differential pairs is the reduced input common-mode range (ICMR). In order to minimize the supply requirements of the input stage, both input terminals of an Op-amp must work with potentials very close to one of the supply rails.

To overcome this limitation, several schemes for discrete time (switched) operation with a single supply down to 1V and large output signal swings have been recently reported. The switched-opamp (SO) technique has been shown to be a promising low-cost solution to realize switched-capacitor (SC) circuits in standard CMOS processes.

The SO eliminates critical MOS switches that set the minimum supply voltage to allow sub-1-V operation[1] of the SC circuits and, thus, does not have a reliability problem. Since then, a few modifications have been proposed to improve the performance of the SO techniques in terms of operation speed and compatibility with existing SC circuits.

1.4 DYNAMIC LATCHED COMPARATOR

The dynamic latched comparator is composed of two stages. The first stage is the interface stage which consists of all the transistors except two cross coupled inverters. The second stage is the regenerative stage that is comprised of the two cross coupled inverters, where each input is connected to the output of the other. It operates in two phases. 1) Interface phase and 2) Regeneration phase. It consists of single nmos tail transistor connected to ground. When clock is low tail transistor is off and depending on V_p and V_n output reaches to VDD or Gnd. When clock is high tail transistor is on and both the outputs discharges to ground. There is reduction of both power and delay in dynamic latched comparator circuit over the double tail latched and pre-amplifier based clocked comparators.

Double tail latched comparator has less power consumption but low speed because of more transistor count and pre-amplifier based clocked comparator has high speed because of less transistor count but power consumption is more because it uses an amplification stage, it consumes static power during the amplification period. However, since the pre-amplifier based clocked comparator is to work at high frequency, the energy consumption of the pre-amplifier based clocked comparator becomes comparable to the double tail latched comparator. Hence the performance of the pre-amplifier based clocked comparator is limited by the static power dissipation in the evaluation or regeneration phase.

1.5 CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch[6]. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset and random decision errors, and kick-back noise. In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

II. EXISTING SYSTEM ANALYSIS

2.1 SINGLE TAIL COMPARATOR

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing[1], and no static power consumption.

During the reset phase when $CLK = 0$ and M_{tail} is off, reset transistors ($M7-M8$) pull both output nodes Out_n and Out_p to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when $CLK = VDD$, transistors $M7$ and $M8$ are off, and M_{tail} is on.

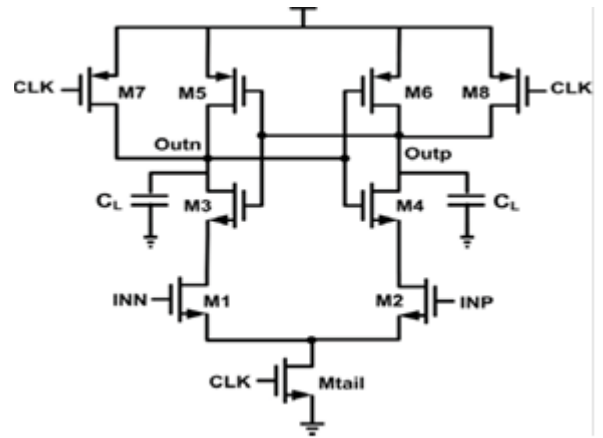


Fig.2. Single Tail Comparator

Output voltages (Out_p , Out_n), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where $V_{INP} > V_{INN}$, Out_p discharges faster than Out_n , if $V_{INP} < V_{INN}$ out_n discharges faster than out_n .

2.2 CONVENTIONAL DYNAMIC COMPARATOR

The schematic diagram of the conventional dynamic comparator widely used in A/D converters[2], with high input impedance, rail-to-rail output swing[10], and no static power consumption[10]. The operation of the comparator is as follows. During the reset phase when $CLK = 0$ and M_{tail} is off, reset transistors ($M7-M8$) pull both output nodes Out_n and Out_p to VDD to define a start condition and to have a valid logical level during reset.

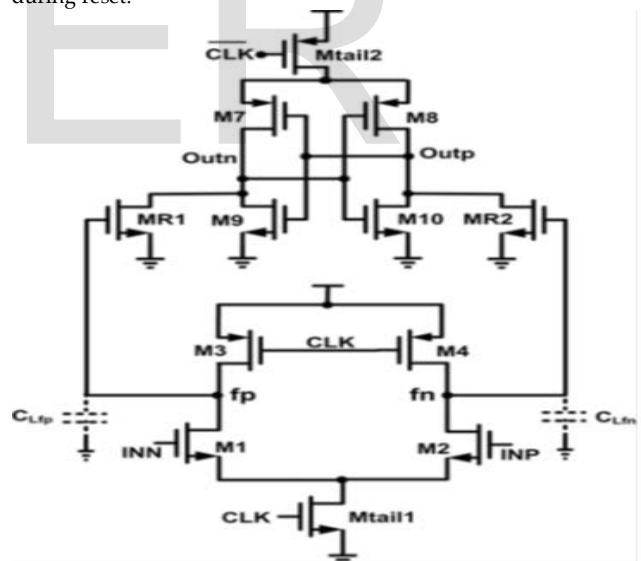


Fig.3. Conventional Dynamic Comparator

In the comparison phase, when $CLK = VDD$, transistors $M7$ and $M8$ are off, and M_{tail} is on. Output voltages (Out_p , Out_n), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where $V_{INP} > V_{INN}$, Out_p discharges faster than Out_n , hence when Out_p (discharged by transistor $M2$ drain current), falls down to $VDD - |V_{thp}|$ before Out_n (discharged by transistor $M1$ drain current), the corresponding pMOS transistor ($M5$) will turn on initiating the latch regeneration caused by back-to-back inverters ($M3, M5$ and $M4, M6$). Thus, Out_n pulls to VDD and Out_p discharges to ground. If $V_{INP} < V_{INN}$, the circuit works vice versa.

The delay of this comparator is comprised of two time delays, t_0 and t_1 Latch. The delay t_0 represents the capacitive discharge of the load capacitance C_L until the first p-channel transistor (M5/M6) turns on.

2.3 OFFSET VOLTAGE ANALYSIS OF DYNAMIC LATCHED COMPARATOR

Due to fast-speed, low-power consumption, high-input impedance and full-swing output, CMOS dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs)[2], memory sense amplifiers (SAs), and data receivers. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) to convert a small input-voltage difference to a full-scale digital level in a short time. However, the accuracy of such comparators is limited by the random offset voltage resulting from the device mismatches such as threshold voltage V_{th} , current factor β ($=\mu C_{ox}W/L$) and internal parasitic/external load capacitance mismatches.

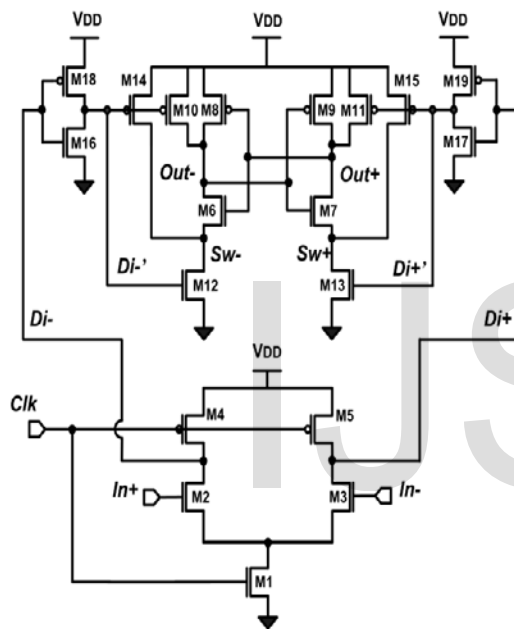


Fig.4.Schematic of the Proposed Comparator

The offset voltage contribution of each stage of the dynamic latched comparator[10] is analyzed and verified with the extracted ones from transient Monte- Carlo simulations. Based on the result, the dynamic latched comparator is designed and optimized. In addition to the optimum design method, a digitally controlled capacitive offset voltage compensation technique is demonstrated to further calibrate the total offset voltage using 90nm PTM technology and 1V power supply voltage[7].

2.3.1 Offset Voltage Analysis Of Dynamic Comparator

The dynamic comparator shown in Figure 4 is used for our offset voltage analysis. During the pre-charge (or reset) phase ($Clk=0V$), both PMOS transistors M4 and M5 turn on and Di nodes' capacitances are charged to VDD, which in turn make both NMOS transistor M16 and M17 of the inverter pair on and Di' nodes discharge to ground. Sequentially, PMOS transistor M10, M11, M14 and M15 turn on and Out nodes and Sw nodes are charged up to VDD while both NMOS transistors M12 and M13 are off.

During evaluation (decision-making) phase ($Clk=VDD$), each Di node capacitance is discharged from VDD to ground in a different rate proportional to the magnitude of each input voltage. As a result, an input

dependent differential voltage is formed between $Di+$ and $Di-$ nodes. Once either $Di+$ or $Di-$ node voltage drops below $VDD-|V_{tp}|$, the inverter pairs (M18/M16 and M19/M17) invert each Di node signal into the regenerated (amplified) Di' node signals. Then the regenerated and different phased Di' node voltages are relayed to the output-latch stage by M10-M13. As the regenerated each Di' node voltage is rising from 0V to VDD with a different time interval, M12 and M13 turn on one after another and the output latch starts regenerating the small voltage difference transmitted from Di' nodes into a full-scale digital level: $Out+$ node will output logic high (VDD) if $Di+$ node voltage is rising faster than $Di-$ node voltage and $Out+$ will output logic low (0V) otherwise. Once either of Out node voltages drops below $VDD-|V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on.

Since the dynamic comparator shown in Figure 1 can be divided into three stages, the total offset voltage ($V_{OS, tot}$) can be expressed as

$$V_{OS, tot} = \sqrt{V_{OS, Diff, Input}^2 + \frac{1}{G_1^2} \cdot V_{OS, Inv. Pair}^2 + \frac{1}{G_1^2 \cdot G_2^2} \cdot V_{OS, Output Latch}^2} \quad (1)$$

Where $V_{OS_different}$ Input $V_{OS_Inv. Pair}$ and $V_{OS_Output Latch}$ are the offset voltages resulting from the mismatched transistor pairs in each stage, respectively[8]. G_1 is the voltage gain between Di nodes and In nodes and G_2 is the voltage gain between Di' nodes and Di nodes.

To optimize the comparator in terms of the minimal offset voltage, the offset voltage contributions of each stage have to be verified first. Therefore, all transistors (but the inverter pairs) are designed to have the same aspect ratio of $W/L=1\mu m/0.1\mu m$. In order for the inverter pair to have the proper gain and correct functionality, PMOS transistors of the inverter pair are designed three times bigger than NMOS transistors ($W_p/W_n=1.5\mu m/0.5\mu m$). To simulate 1-sigma offset voltages for each stage, the random mismatch[7][6] in threshold voltage V_{th} and current factor β ($=\mu C_{ox}W/L$) for each transistor pair are modeled as follows,

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}}, \quad \sigma_{\beta} = \frac{A_{\beta}}{\sqrt{WL}} \quad \text{where } W, L \text{ are in } \mu m \quad (2)$$

$A_{V_{th}}$ and A_{β} are process dependent parameters and are assumed to be $4.5mV \cdot \mu m$ and $1\% \cdot \mu m$, respectively in this mismatch analysis. As shown in Figure 2 (in Grey), the input referred offset voltages of each stage of the comparator with respect to the different the input common mode voltages are extracted from 100 times of transient Monte-Carlo simulations ($VDD=1V, f_{clk}=3GHz$). As expected, the offset voltage resulting from the mismatched transistor pairs in the regenerative output-latch stage is the smallest.

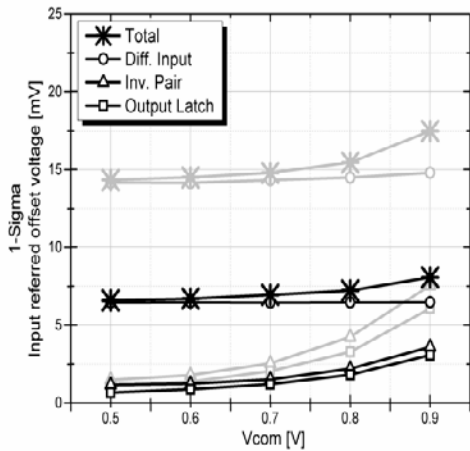


Fig.5. Offset Voltage Contributions of each stage before and after Optimization.

since it is reduced by the gain of $G1 \times G2$ and the offset voltage from the mismatch between the inverter pair, which is reduced by the gain of $G1$, is also small comparing to the offset voltage of the differential input stage. The offset voltage of the differential input stage can be approximated.

III. PROPOSED SYSTEM ANALYSIS

3.1 DOUBLE-TAIL DYNAMIC COMPARATOR

Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase V_{fn}/f_p in order to increase the latch regeneration speed.

For this purpose, two control transistors (MC1 and MC2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner. During compare than existing, proposed double tail comparator is efficient Power consumption and delay is efficient than existing.

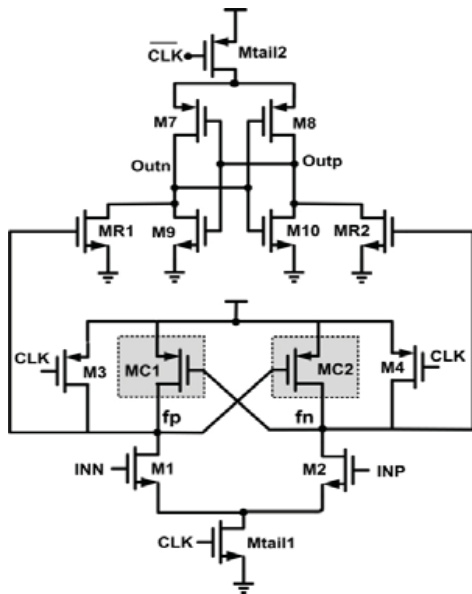


Fig.6. Proposed Double Tail Dynamic Comparator

TABLE I
SUMMARY OF THE COMPARATOR PERFORMANCE

Item	Value
Technology	180-nm CMOS
Supply voltage	1.2 V
Average power dissipation per conversion @ freq.=500 MHz	329 μ W
Worst case delay ($V_{cm}=0.6$ V, $\Delta V_{in}=1$ mV)	550 ps
Delay / $\log(\Delta V_{in})$	69 ps/dec
Offset standard deviation (1-signal) (σ_{os})	7.8 mV
Energy efficiency	0.66 pJ

IV. EXPERIMENTAL RESULT

In order to compare the proposed comparator with the conventional and double-tail dynamic comparators, all circuits have been simulated in a 0.18- μ m CMOS technology

INCREASED IN LEAKAGE CURRENT

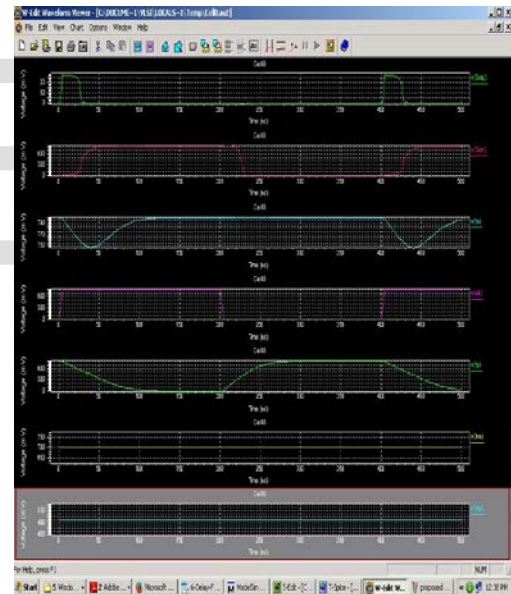


Fig.7. Simulation Result For increased in Leakage Current

The leakage current in the increased will be more due to the separation of sensing and slave latch circuit. It leads to wastage of more current.

DECREASED IN LEAKAGE CURRENT

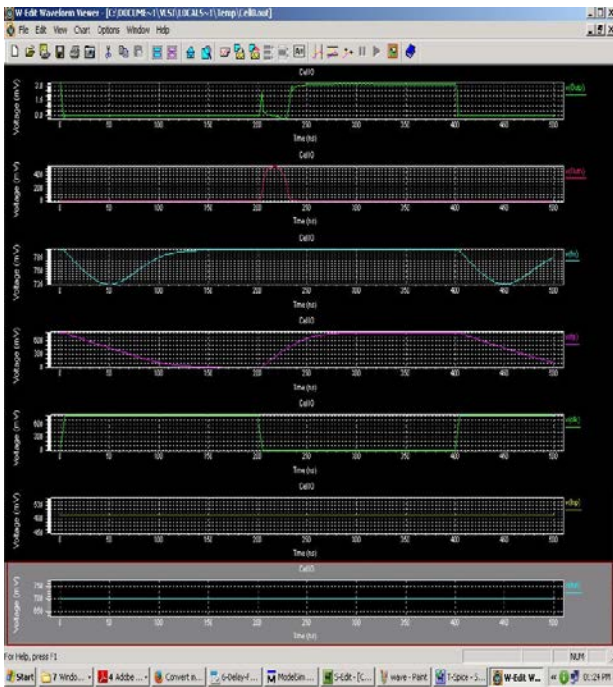


Fig.8. Simulation Result For decreased Leakage Current

The leakage current in the decreased will be more due to the separation of sensing and slave latch circuit. It leads to wastage of more current.

TABLE II
COMPARISON FOR EXISTING AND PROPOSED COMPARATOR

Process	Power	Delay
Single Tail Comparator	7.04×10^{-6} = $7 \mu\text{W}$	6.61×10^{-8} = 66ns
Conventional Double Tail Comparator	1.50×10^{-5} = $15 \mu\text{W}$	7.50×10^{-9} = 7.5ns
Proposed Double Tail Comparator	1.29×10^{-5} = $12 \mu\text{W}$	7.40×10^{-9} = 7.4ns

V.CONCLUSION

In this work presented a comprehensive delay analysis for clocked dynamic comparators. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to

improve the performance of the comparator. Post-layout simulation results in 0.18- μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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